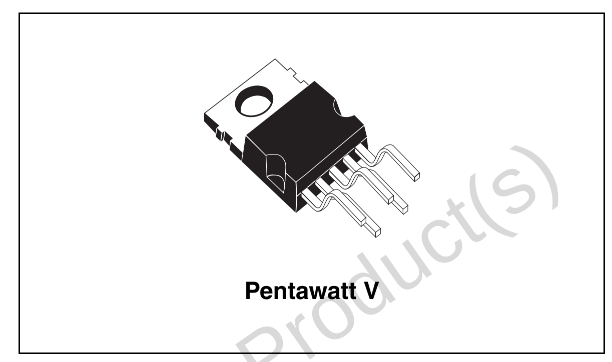


TDA2050

32 W hi-fi audio power amplifier

Features

- High output power (50 W music power IEC 268.3 rules)
- High operating supply voltage (50 V)
- Single or split supply operations
- Very low distortion
- Short-circuit protection (OUT to GND)
- Thermal shutdown



Description

The TDA 2050 is a monolithic integrated circuit in a Pentawatt package, intended for use as an audio class-AB audio amplifier.

Thanks to its high power capability the TDA2050 is able to provide up to 35 W true RMS power into a 4 ohm load at THD = 0%, V_S = ±18 V, f = 1 kHz and up to 32 W into an 8 ohm load at THD = 10%, V_S = ±22 V, f = 1 kHz.

Moreover, the TDA2050 delivers typically 50 W music power into a 4 ohm load over 1 sec at V_S = 22.5 V, f = 1 kHz.

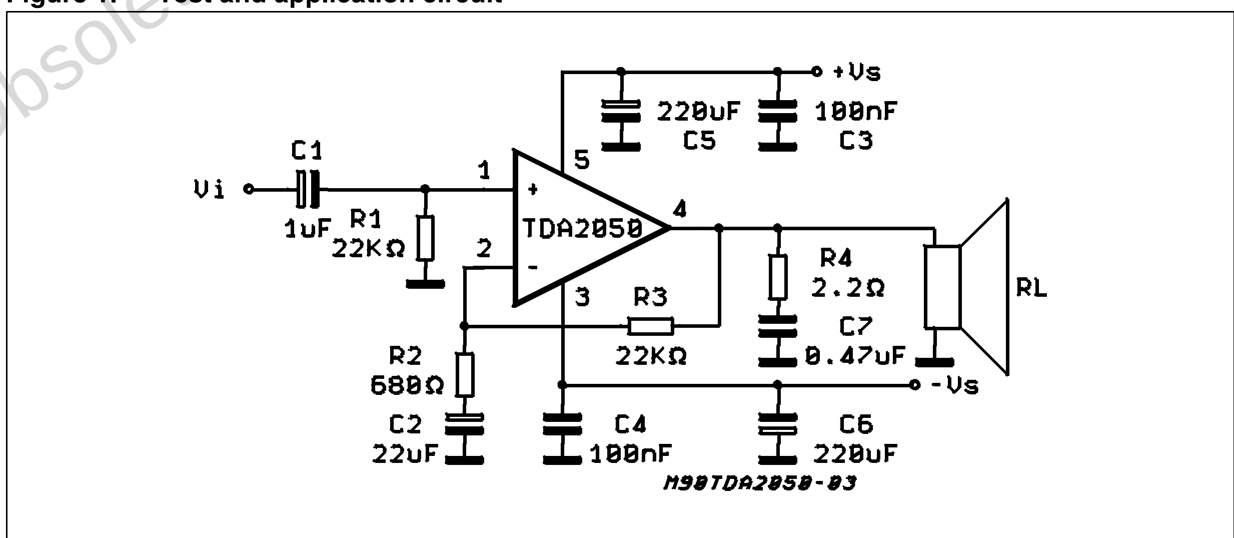
The high power and very low harmonic and crossover distortion (THD = 0.05% typ, at V_S = ±22 V, P_O = 0.1 to 15 W, R_L = 8 ohm, f = 100 Hz to 15 kHz) make the device most suitable for both hi-fi and high-end TV sets.

Table 1. Device summary

Order code	Package
TDA2050V	Pentawatt vertical



Figure 1. Test and application circuit



1 Device overview

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage	±25	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	±15	V
I_o	Output peak current (internally limited)	5	A
P_{tot}	Power dissipation at T_{CASE} = 75 °C	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	3 (max)	°C

Figure 2. Pin connections (top view)

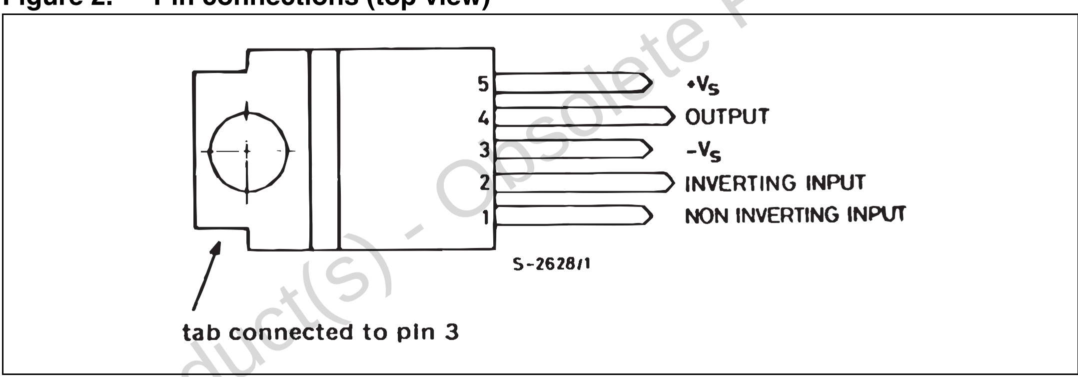
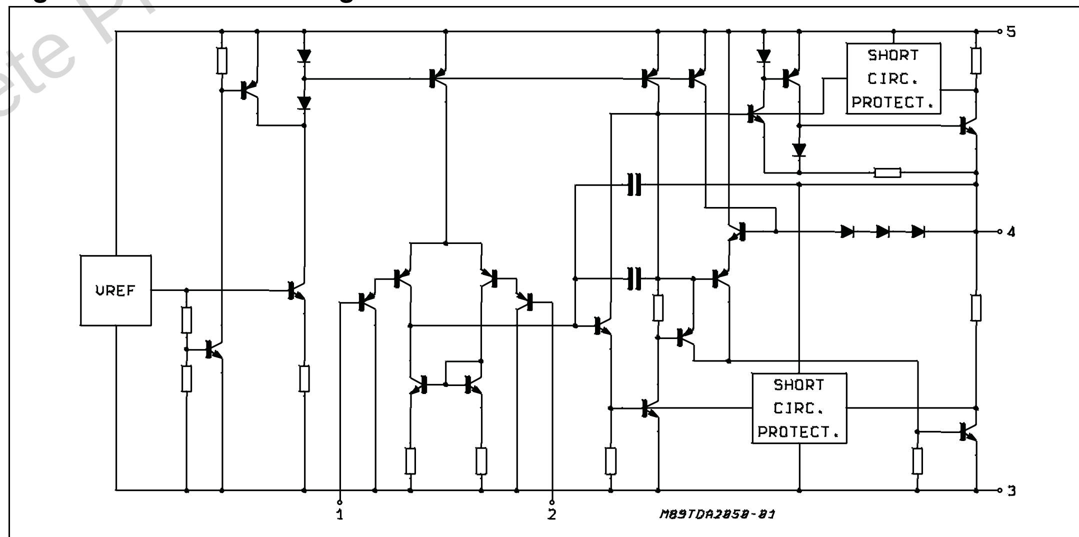


Figure 3. Schematic diagram



The values given in the following table refer to the test circuit V_S = ±18 V, T_{amb} = 25 °C, f = 1 kHz, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		± 4.5		± 25	V
I_d	Quiescent drain current	V_s = ± 4.5 V_s = ± 25		30 55	50 90	mA mA
I_b	Input bias current	V_s = ± 22		0.1	0.5	µA
V_{OS}	Input offset voltage	V_s = ± 22			± 15	mV
I_{OS}	Input offset current				± 200	nA
P_O	Output power	d = 0.5%, R_L = 4 Ω R_L = 8 Ω V_s = ± 22 V, R_L = 8 Ω	 24 22	 28 18 25		 W W W
		d = 10%, R_L = 4 Ω R_L = 8 Ω V_s = ± 22 V, R_L = 8 Ω		 35 22 32		 W W W
	Music power IEC268.3 rules	d = 10%, T = 1s R_L = 4 Ω; Vs = ± 22.5 V		50		W
d	Distortion	P_o = 0.1 to 24W, R_L = 4 Ω, f = 1 kHz f = 100 to 10 kHz, Po = 0.1 to 18 W		0.03	0.5 0.5	% %
		Vs = ± 22 V, R_L = 8 Ω, f = 1 kHz, Po = 0.1 to 20 W, f = 100 Hz to 10 kHz; P_o = 0.1 to 15 W		0.02	 0.5	% %
SR	Slew rate		5	8		V/µs
G_V	Voltage gain (open loop)	f = 1 kHz		80		dB
G_V	Voltage gain (closed loop)	f = 1 kHz	30	30.5	31	dB
BW	Power bandwidth (-3dB)	V_i = 200 mW, R_L = 4 Ω;		20 to 80.000		Hz
e_N	Input noise voltage	B = Curve A B = 22 Hz to 22 kHz		4 5	 10	µV µV
R_i	Input resistance (pin 1)		500			kΩ
SVR	Supply voltage rejection	R_g = 22 kΩ, f = 100 Hz; V_{ripple} = 0.5 V_{RMS}		45		dB
h	Efficiency	P_o = 28 W, R_L = 4 Ω		65		%
		P_o = 25 W, R_L = 8 Ω,V_s = ± 22 V,		67		%
$T_{sd\text{-}j}$	Thermal shutdown junction temperature			150		°C

Figure 4. Split-supply typical application circuit

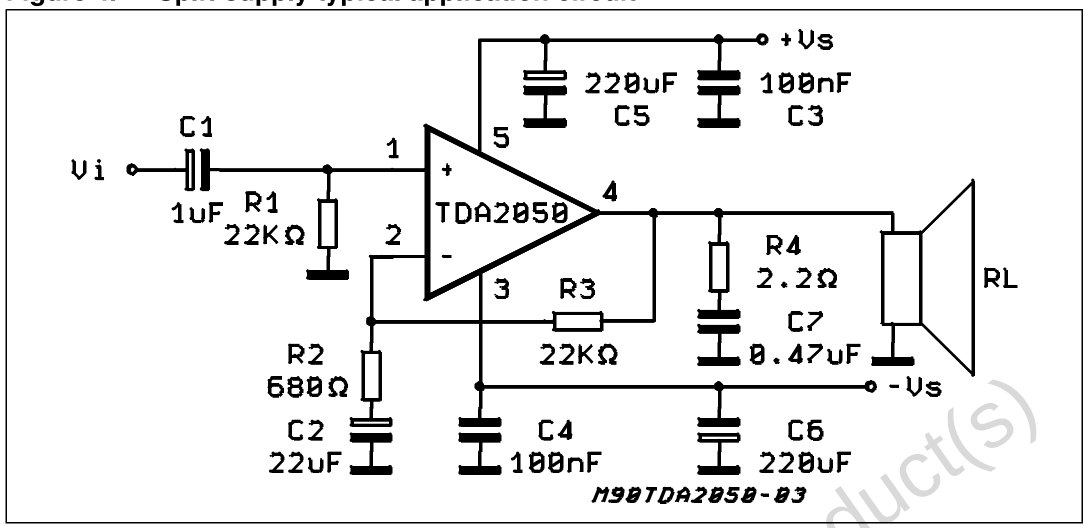
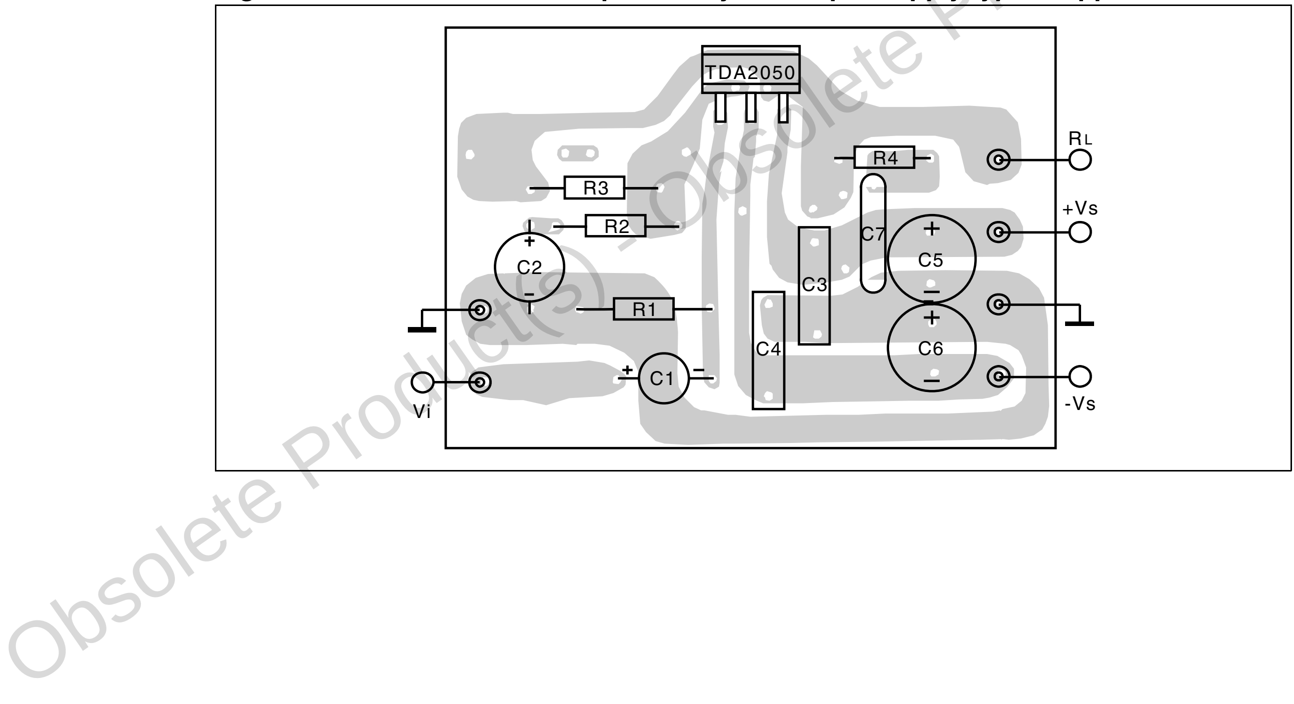


Figure 5. PC board and component layout of split-supply typical application circuit



2 Split-supply application suggestions

The recommended values of the external components are those shown on the application circuit of *Figure 5*. Different values can be used. The following table can help the designer.

Table 5. Recommended values of external components

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Input impedance	Increase of input impedance	Decrease of Input Impedance
R2	680 Ω	Feedback resistor	Decrease of gain(1)	Increase of gain
R3	22 kΩ		Increase of gain	Decrease of gain(1)
R4	2.2 Ω	Frequency stability	Danger of oscillations	
C1	1 µF	Input decoupling DC		Higher low-frequency cutoff
C2	22 µF	Inverting input DC decoupling	Increase of switch ON/OFF noise	Higher low-frequency cutoff
C3, C4	100 nF	Supply voltage bypass		Danger of oscillation
C5, C6	220 µF	Supply voltage bypass		Danger of oscillation
C7	0.47 µF	Frequency stability		Danger of oscillation

1. The gain must be higher than 24 dB

2.1 Printed circuit board

The layout shown in *Figure 5* should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Figure 6. Single-supply typical application circuit

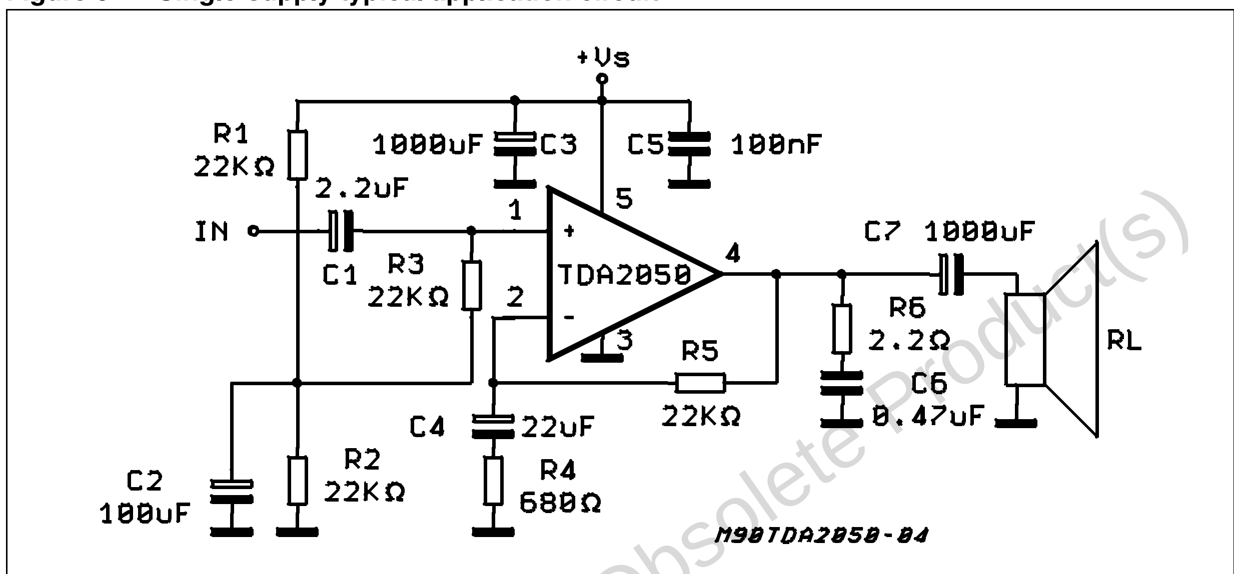
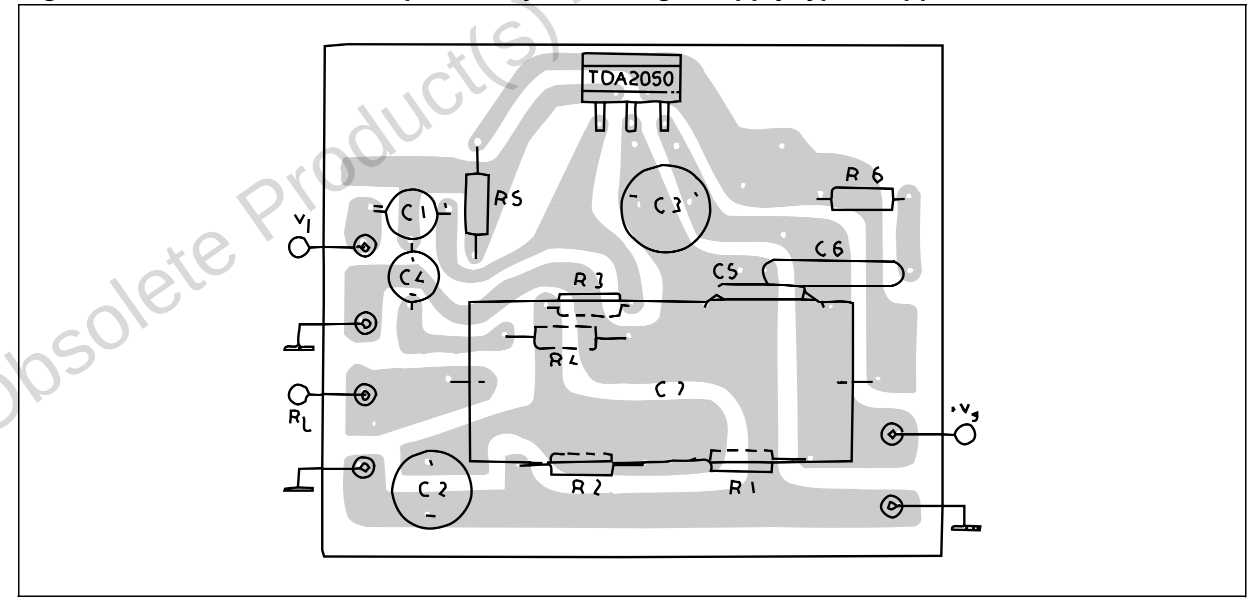


Figure 7. PC board and component layout of single-supply typical application circuit



3 Single-supply application suggestions

The recommended values of the external components are those shown in the application circuit of *Figure 6*. Different values can be used. The following table can help the designer.

Table 6. Recommonded values

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R1, R2, R3	22 kΩ	Biasing resistor		
R4	680 Ω	Feedback resistor	Increase of gain	Decrease of gain[1]
R5	22 kΩ		Decrease of gain[1]	Increase of gain
R6	2.2 Ω	Frequency stability	Danger of oscillations	
C1	2.2 µF	Input decoupling DC		Higher low-frequency cutoff
C2	100 µF	Supply voltage rejection	Worse turn-off transient Worse turn-on delay	
C3	1000 µF	Supply voltage bypass		Danger of oscillations Worse turn-off transient
C4	22 µF	Inverting input DC decoupling	Increase of switching ON/OFF	Higher low-frequency cutoff
C5	100 nF	Supply voltage bypass		Danger of oscillations
C6	0.47 µF	Frequency stability		Danger of oscillations
C7	1000 µF	Output DC decoupling		Higher low-frequency cutoff

1. The gain must be higher than 24 dB

Note: If the supply voltage is lower than 40 V and the load is 8 ohm (or more), a lower value of C2 can be used (i.e. 22 mF). C7 can be larger than 1000 µF only if the supply voltage does not exceed 40 V.

4 Typical characteristics (split-supply test circuit unless otherwise specified)

Figure 8. Output power vs. supply voltage

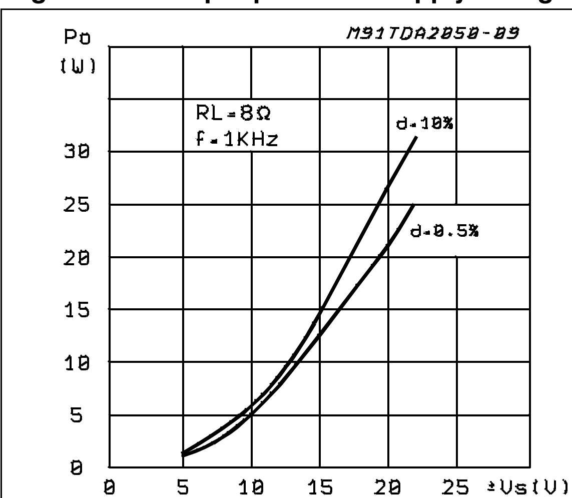


Figure 9. Distortion vs. output power

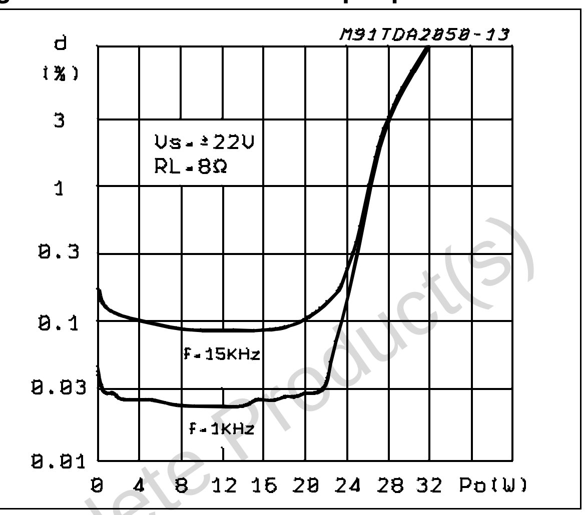


Figure 10. Output power vs. supply voltage

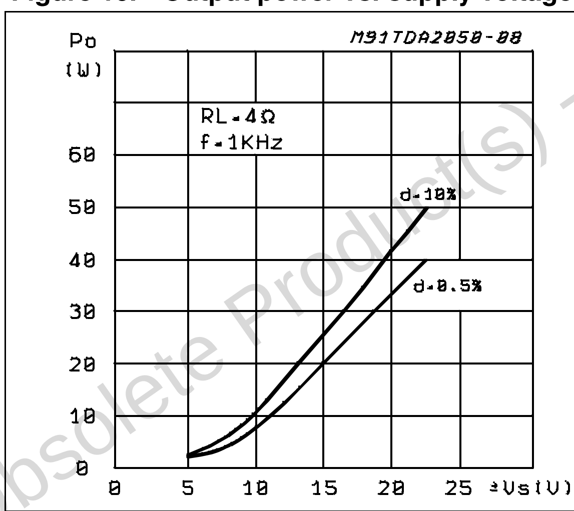


Figure 11. Distortion vs. output power

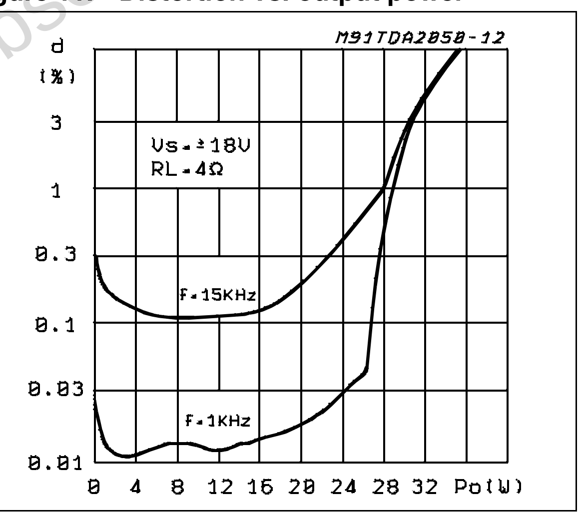


Figure 12. Distortion vs. frequency

Figure 13. Distortion vs. frequency

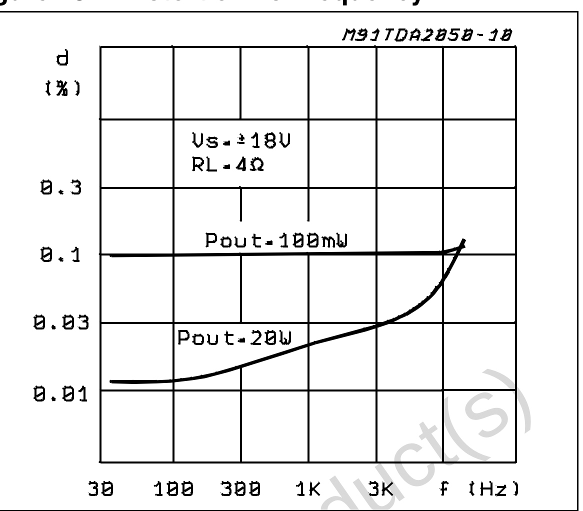


Figure 14. Quiescent current vs. supply voltage

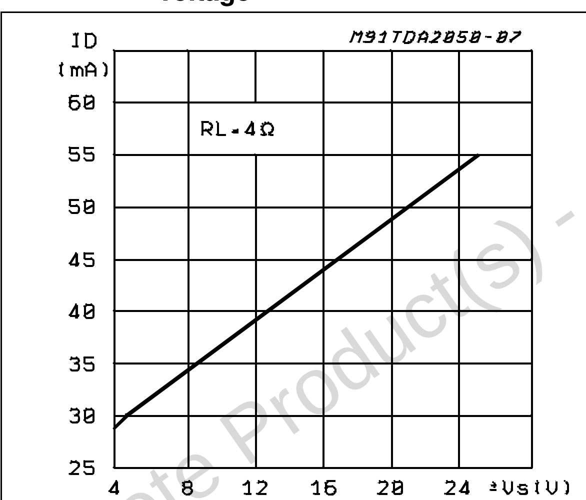


Figure 15. Supply voltage rejection vs. frequency

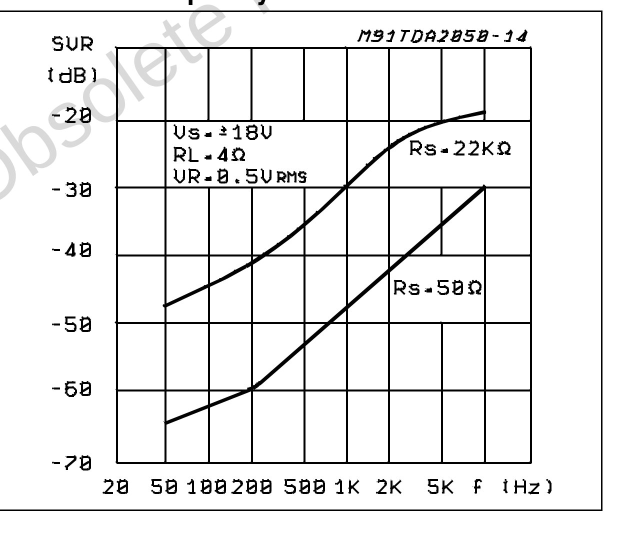


Figure 16. Supply voltage rejection vs. frequency (single-supply) for different values of C2 (*Figure 6*)

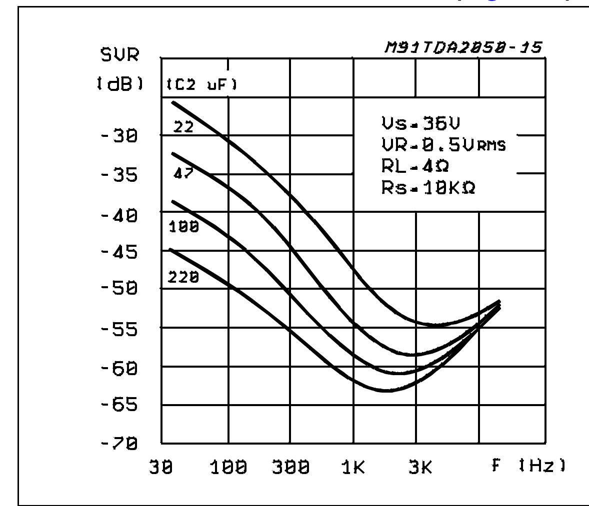


Figure 17. Supply voltage rejection vs. frequency (single-supply) for different values of C2 (*Figure 6*)

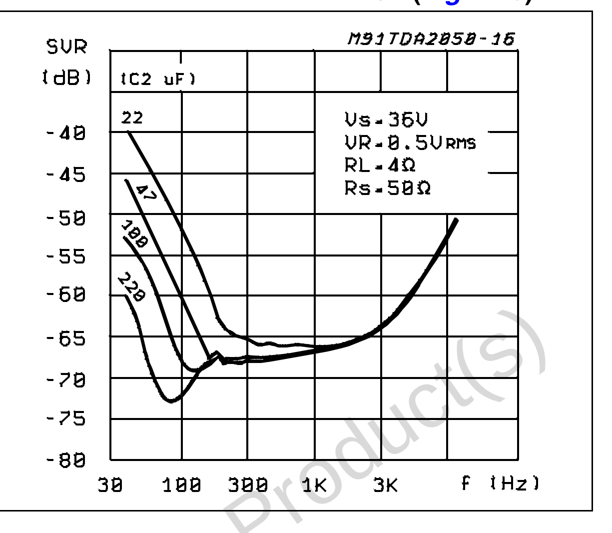


Figure 18. Total power dissipation and efficiency vs. output power

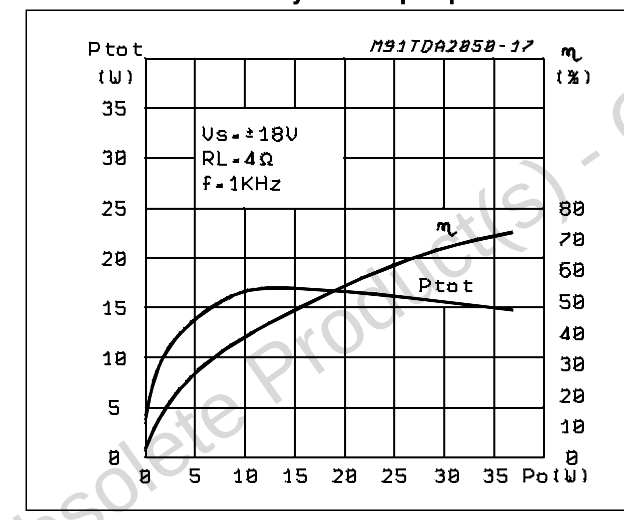
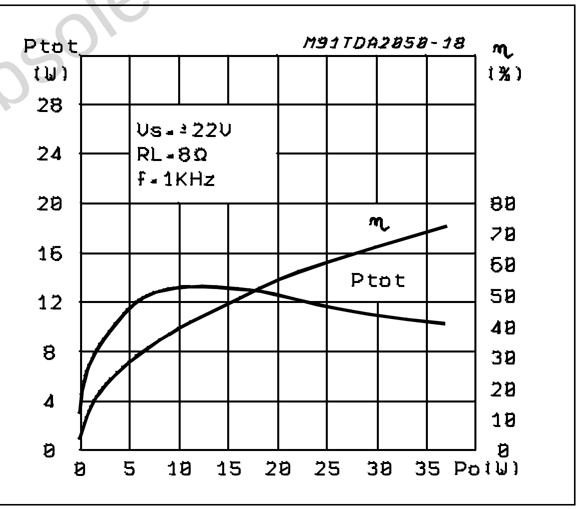


Figure 19. Total power dissipation and efficiency vs. output power



5 Short-circuit protection

The TDA2050 has an original circuit which limits the current of the output transistors. The maximum output current is a function of the collector emitter voltage, hence the output transistors work within their safe operating area. This function can therefore be considered as being peak power limiting rather than simple current limiting. It reduces the possibility that the device gets damaged during an accidental short-circuit from AC output to ground.

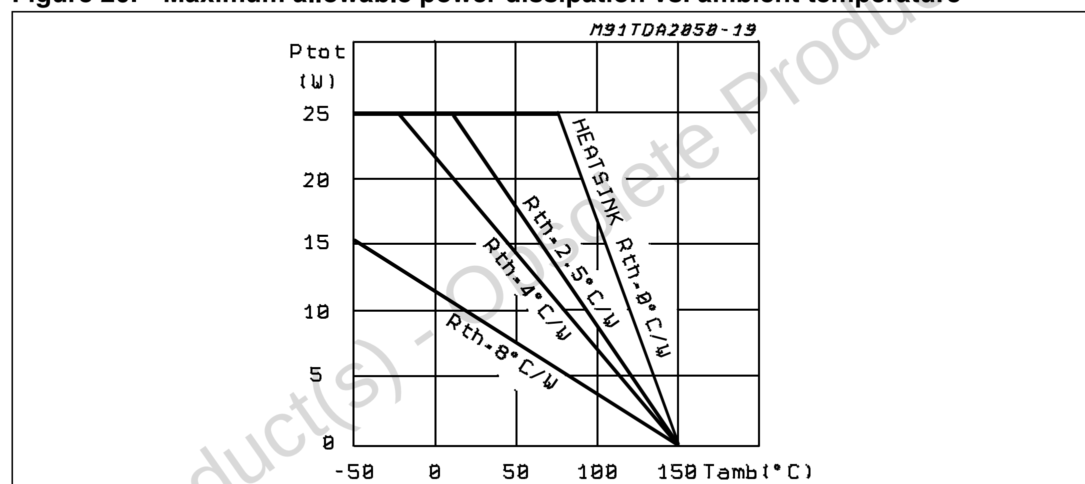
6 Thermal shutdown

The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily tolerated since Tj cannot be higher than 150 °C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150 °C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the thermal resistance junction-ambient. *Figure 20* shows this dissipable power as a function of ambient temperature for different thermal resistances.

Figure 20. Maximum allowable power dissipation vs. ambient temperature



6.1 Mounting instructions

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the pentawatt package, the heatsink mounting operation is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces. *Figure 21* shows an example of a heatsink.

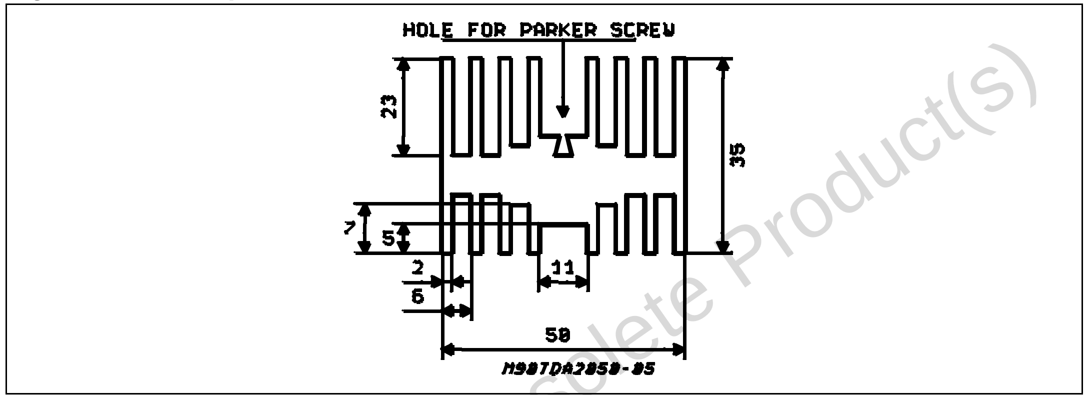
6.2 Dimension recommendations

The following table shows the length that the heatsink in *Figure 21* must have for several values of P_{tot} and R_{th}.

Table 7. Dimension recommendations

P_{tot} (W)	12	8	6
Length of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

Figure 21. Example of heatsink



Appendix A

A.1 Music power concept

Music power is (according to the IEC clauses n.268-3 of Jan. 83) the maximum power which the amplifier is capable of producing across the rated load resistance (regardless of non-linearity) 1 sec after the application of a sinusoidal input signal of frequency 1 kHz.
According to this definition our method of measurement comprises the following steps:

- Set the voltage supply at the maximum operating value
- Apply a input signal in the form of a 1 kHz tone burst of 1 sec duration: the repetition period of the signal pulses is 60 sec
- The output voltage is measured 1 sec from the start of the pulse
- Increase the input voltage until the output signal shows a THD=10%
- The music power is then V^2_{out}/R_L, where V_{out} is the output voltage measured in the condition of point 4 and R_L is the rated load impedance

The target of this method is to avoid excessive dissipation in the amplifier.

A.2 Instantaneous power

Another power measurement (maximum instantaneous output power) was proposed by the IEC in 1988 (IEC publication 268-3 subclause 19.A). We give here only a brief extract of the concept, and a circuit useful for the measurement. The supply voltage is set at the maximum operating value.

The test signal consists of a sinusoidal signal whose frequency is 20 Hz, to which are added alternate positive and negative pulses of 50 µs duration and 500 Hz repetition rate. The amplitude of the 20 Hz signal is chosen to drive the amplifier to its voltage clipping limits, while the amplitude of the pulses takes the amplifier alternately into its current-overload limits. A circuit for generating the test signal is given in *Figure 22*.

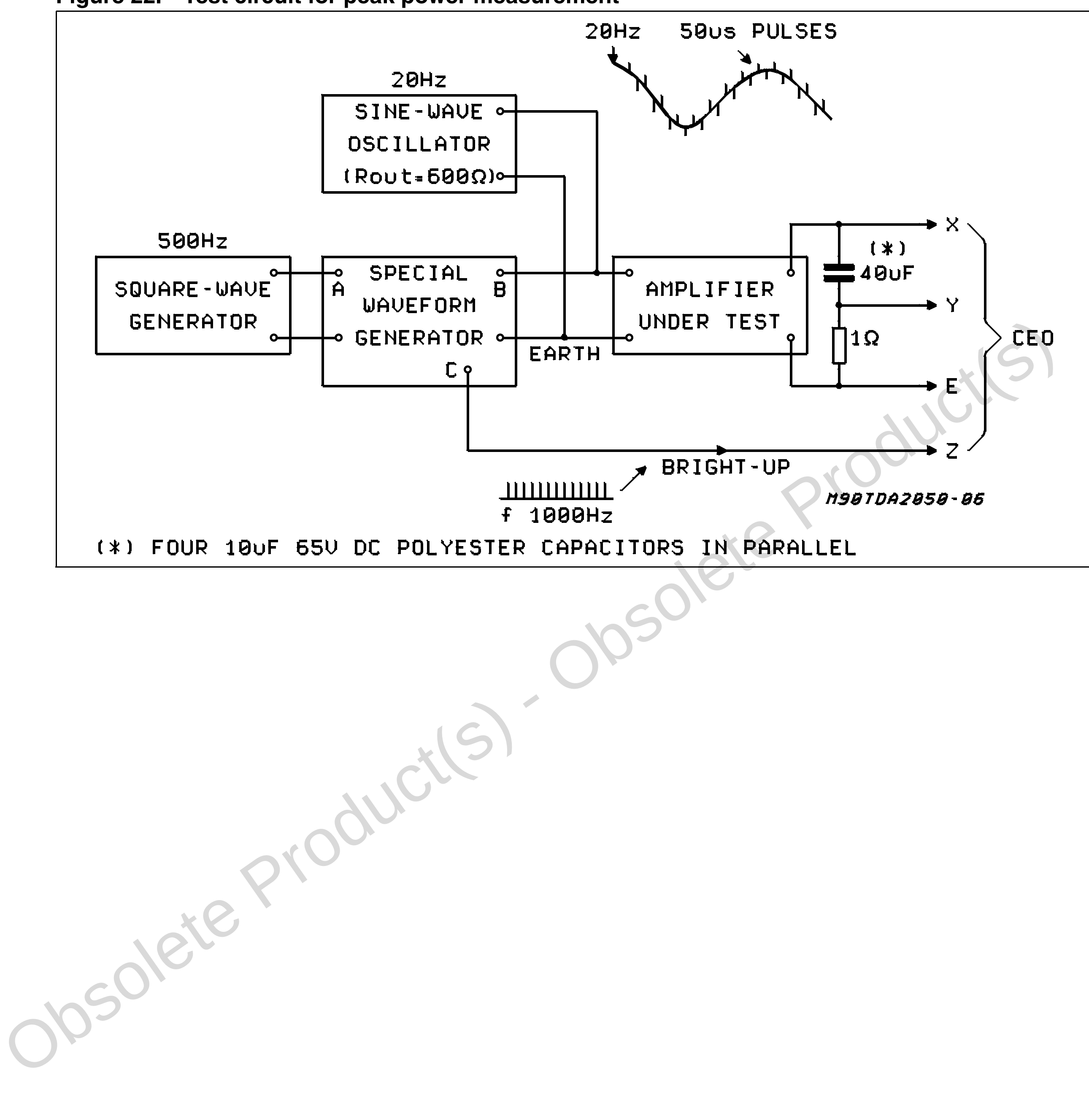
The load network consists of a 40 µF capacitor, in series with a 1 ohm resistor. The capacitor limits the current due to the 20 Hz signal to a low value, whereas for the short pulses the effective load impedance is of the order of 1 ohm, and a high output current is produced.

Using this signal and load network the measurement may be made without causing excessive dissipation in the amplifier. The dissipation in the 1 ohm resistor is much lower than a rated output power of the amplifier, because the duty-cycle of the high output current is low. By feeding the amplifier output voltage to the Xplates of an oscilloscope, and the voltage across the 1 ohm resistor (representing the output current) to the Y=plates, it is possible to read on the display the value of the maximum instantaneous output power.

The result of this test applied on the TDA2050 is:

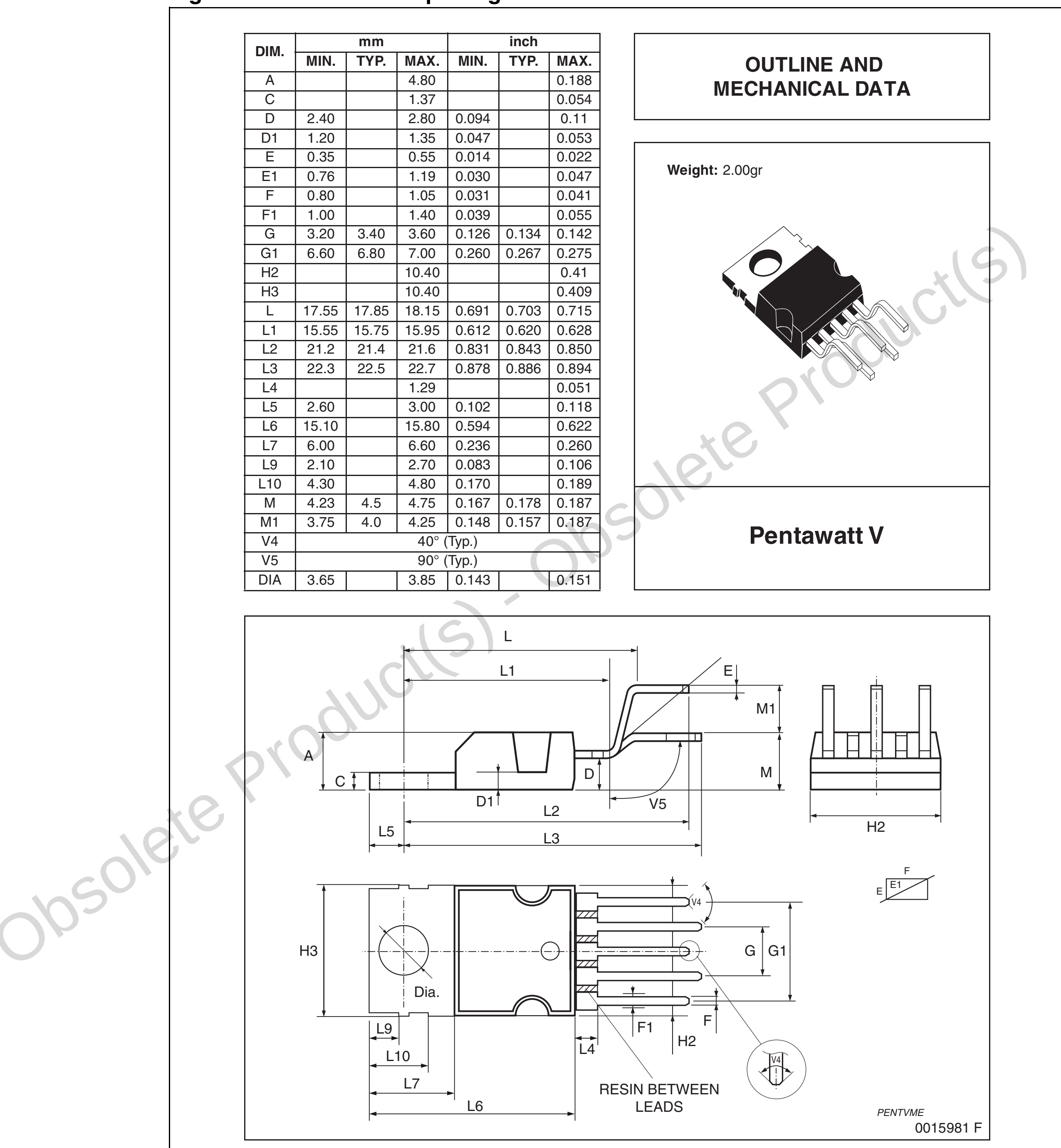
Peak power = 100 W typ

Figure 22. Test circuit for peak power measurement



7 Package mechanical data

Figure 23. Pentawatt V package



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.80			0.188
C			1.37			0.054
D	2.40		2.80	0.094		0.11
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.76		1.19	0.030		0.047
F	0.80		1.05	0.031		0.041
F1	1.00		1.40	0.039		0.055
G	3.20	3.40	3.60	0.126	0.134	0.142
G1	6.60	6.80	7.00	0.260	0.267	0.275
H2			10.40			0.41
H3			10.40			0.409
L	17.55	17.85	18.15	0.691	0.703	0.715
L1	15.55	15.75	15.95	0.612	0.620	0.628
L2	21.2	21.4	21.6	0.831	0.843	0.850
L3	22.3	22.5	22.7	0.878	0.886	0.894
L4			1.29			0.051
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
L9	2.10		2.70	0.083		0.106
L10	4.30		4.80	0.170		0.189
M	4.23	4.5	4.75	0.167	0.178	0.187
M1	3.75	4.0	4.25	0.148	0.157	0.187
V4	40° (Typ.)					
V5	90° (Typ.)					
DIA	3.65		3.85	0.143		0.151

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
31-Aug-2011	3	Removed minimum value from Pentawatt (vertical) package dimension H3 in *Figure 23: Pentawatt V package* Revised general presentation, minor textual updates

